AMENDMENTS TO THE CLAIMS

Claim 1 (currently amended): An A/D converter, comprising:

a plurality of capacitors and at least one comparator, arranged to perform an analog to digital conversion of an analog input signal to a digital output signal; ~~and~~

a plurality of level latches;

a control circuit, controlling said plurality of level latches; ~~capacitors to be used for both analog to digital conversion and for calibration.~~

wherein

said plurality of capacitors are used for both analog to digital conversion and for calibration,

said control circuit stores in said plurality of level latches levels associated with calibration, and

said plurality of level latches are connected to control a level applied to respective bottom plates of said capacitors.

Claims 2-3 (cancel):

Claim 4 (currently amended) The converter as in claim 1, ~~2,~~ wherein said ~~control circuit controls a level which is supplied to a bottom plate of each said capacitor, and wherein~~ a top plate of each said capacitor is connected together to form a common line.

Claim 5 (currently amended) The converter as in claim 1, ~~2,~~ further comprising an image acquisition element, obtaining information indicative of a portion of an image, and producing an output indicative thereof, said an output being analog to digitally converted by said analog to digital converter.

Claim 6 (previously presented) The converter as in claim 4, wherein said level supplied to a bottom plate of each said capacitors can be one of two different voltage levels or a ground level.

Claim 7 (cancel)

Claim 8 (previously presented) The converter as in claim 5, wherein said image acquisition element is a MOS element.

Claim 9 (previously presented) The converter as in claim 8, wherein said image acquisition element is one of a MOS photo diode or a MOS photo gate, and forms an active pixel sensor.

Claims 10-11 (cancel)

Claim 12 (currently amended) The converter as in claim 1, ~~10,~~ wherein said level can be one of ground or a single voltage level.

Claim 13 (cancel)

Claim 14 (currently amended) The converter as in claim 1, ~~13,~~ wherein said level latches store a negative version of a calibration level.

Claim 15 (previously presented) The converter as in claim 14, wherein said negative version is stored in said level latches in a two's compliment format.

Claim 16 (previously presented) An A/D converter comprising:

a plurality of capacitors, each associated with a specified bit of the digital signal, and each having a top plate connected to a common line and a bottom plate, and a comparator, connected to receive said common line as an output of said capacitor at one input, and a signal at another input; and

a plurality of value latches, each storing a value, and each associated with one of said plurality of capacitors, and changing a value applied to said bottom plate of said capacitor;

wherein the same said capacitors are used both for calibration and for A/D conversion.

Claim 17 (previously presented) The converter as in claim 16, wherein said latches store either a one or a zero, and apply either a ground level or a reference level to said capacitor bottom plates depending on the value stored by said latches.

Claim 18 (previously presented) The converter as in claim 16, further comprising a control circuit, controlling said value latches to store a calibration value, and use said calibration value during analog to digital conversion.

Claim 19 (cancelled)

Claim 20 (previously presented) The converter as in claim 17, wherein said reference level includes two reference levels, one higher than the other.

Claim 21 (previously presented) The converter as in claim 17, wherein said reference level includes a single reference level.

Claim 22 (previously presented) The converter as in claim 17, further comprising a switch, controlled by a level in said latch, and selectively providing either a ground level or a reference level to said capacitor.

Claim 23 (previously presented) The converter as in claim 18, further comprising an image sensing element, producing an output signal indicative of a portion of said image, said output signal being coupled to said plurality of capacitors and comparator to be A/D converted thereby.

Claim 24 (previously presented) The converter as in claim 23, wherein said image sensing element is an element formed of MOS elements.

Claim 25 (previously presented) The converter as in claim 23, wherein said image sensing element is an active pixel sensor, having a photoreceptor, a follower associated with said photoreceptor, and a selector which allows electronic selection, also associated with said photoreceptor.

Claim 26 (previously presented) The converter as in claim 25, wherein said image sensing element is one of a photo diode or a photo gate.

Claim 27 (previously presented) The converter as in claim 25, wherein said follower and said selector are each formed using CMOS elements.

Claim 28 (previously presented) The converter as in claim 27, wherein said value latches are each formed using CMOS elements.

Claim 29 (previously presented) The converter as in claim 28, wherein said value latches, said comparator and said capacitors, and a plurality of said image sensing elements, are each formed on a common substrate.

Claim 30 (previously presented) The converter as in claim 18, wherein said value latches are formed of CMOS elements.

Claim 31 (previously presented) The converter as in claim 18, wherein said value latches store a value calibration value.

Claim 32 (previously presented) The converter as in claim 18, wherein said value latches store a negative of a calibration value.

Claim 33 (currently amended) A method, comprising:

calibrating an A/D converter using a plurality of first capacitors, each having a top plate and a bottom plate;

obtaining a signal to be converted by said A/D converter; and

converting said signal to a digital signal; ~~using at least a plurality of first capacitors for said converting.~~

wherein said converting uses the plurality of said first capacitors by supplying the signal to be converted to the top plates of said first capacitors while setting respective levels of said bottom plates of said first capacitors based on a respective plurality of calibration levels from said calibration.

Claim 34 (currently amended) The method as in claim 33, ~~further comprising obtaining values associated with said calibrating, and storing said values in a memory.~~ wherein said calibration levels are stored in a memory.

Claim 35 (previously presented) The method as in claim 34, wherein said memory includes a plurality of bits associated with said capacitors, each bit storing a value which adjusts a level that is applied to each said capacitor.

Claim 36-37 (cancel)

Claim 38 (previously presented) The method as in claim 33, further comprising storing a calibration level obtained during said calibrating, and using the stored calibration level to apply a calibration level to at least one of said capacitors based on a level of said calibration.

Claim 39 (currently amended) The method as in claim 38, wherein levels of said bottom plates include[[s]] a single reference level and a ground level.

Claim 40 (cancel)

Claim 41 (previously presented) The method as in claim 33, further comprising obtaining a signal indicative of a portion of an image, and using said signal for said converting.

Claim 42 (previously presented) The method as in claim 41, wherein said obtaining a signal comprises attaining a signal on the-same substrate as said A/D converter.

Claims 43-44 (cancel)

Claim 45 (previously presented) The method as in claim 33, wherein said calibrating further comprising obtaining a complement of a calibration level and storing said complement in a plurality of latch elements.

Claim 46 (cancel) The method as in claim 33, further comprising storing a level associated with said calibrating in a plurality of latch elements, associating each of said latch elements with one of said first capacitors, and using said values to adjust a level on said capacitors according to a calibration level, during obtaining a signal.

Claim 47 (currently amended) A method, comprising:

obtaining a value indicative of calibration of an A/D converter using a plurality of capacitors to obtain said value;

storing said value in a latch associated with the A/D converter; and

converting an input value using said plurality of capacitors; ~~, and using said value stored in said latch.~~

wherein

said value stored in said latch is a multiple bit value,

each bit of said multiple bit value respectively associated with, and for controlling a level of a bottom plate of, an individual one of said plurality of capacitors.

Claim 48-50 (cancel)

Claim 51 (previously presented) The method as in claim 47, wherein said input value is a value indicative of a portion of an image.

Claim 52 (currently amended) An active pixel sensor, comprising:

a semiconductor substrate, having a plurality of items formed thereon, said items including:

an image acquisition element, formed using MOS formation technology, and having an MOS follower associated therewith and an MOS selection transistor associated therewith, said image acquisition element producing an output signal indicative thereof; and

an A/D converter element, also formed using MOS formation technology, including a plurality of capacitors and a comparator, said plurality of capacitors

operating both to calibrate said A/D converter element and to convert signals applied to said A/D converter element, the same capacitors being used both for said calibration ~~calibrate~~ and for said conversion, ~~converter,~~ and further comprising a latch, having a plurality of digital storage portions, each formed of CMOS, and each storing a value based on said calibration, ~~calibrate,~~ said values used for setting a level of a bottom plate of said plurality of capacitors. ~~allowing said A/D converter to acquire signals~~.

Claim 53 (previously presented) The sensor as in claim 52, wherein said A/D converter is a successive approximation A/D converter.